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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/712,996	11/17/2003	Shinichi Shuto	XA-9974	9398

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MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
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MCLEAN, VA 22102-3833

EXAMINER	
BAE, JI H	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 03/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/712,996	SHUTO ET AL.	
	Examiner	Art Unit	
	Ji H. Bae	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11-17-2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 16-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 16 recites the limitation "the first external terminal" in line 10 and "said second terminal" in line 14. There is insufficient antecedent basis for this limitation in the claim. There is no prior recitation of a first external terminal or a second terminal.

Claims 17 and 18 are rejected by virtue of their dependency.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 4, 6, 8-11, and 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art [AAPA][1] in view of Hadderman, U.S. Patent No. 5,805,473.

Regarding claim 1, AAPA teaches:

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[1] Japanese Unexamined Patent Application Publication 2000-99215

a semiconductor processing system comprising an interface control circuit and a processing circuit, and attached to an external apparatus so as to receive an operation power supply therefrom, wherein said interface control circuit, when said system is removed from the external apparatus, detects a potential change that occurs at a first external terminal to be disconnected from a predetermined terminal of the external apparatus before the power supply from the external apparatus is shut off [applicant's specification, pages 1-2, "Background of the invention", also translated Patent Abstract, and Fig. 1, 3, 4, 5 of Japanese Patent Application].

AAPA does not teach that the processing circuit is instructed to end processing upon detection that a power supply is shut off.

Hadderman teaches a PCMCIA card configured to detect a loss of voltage, at which time the card causes a processing circuit to end processing upon detection that a power supply is disconnected [col. 7, lines 7-10, Fig. 4, step 405].

It would have been obvious to one of ordinary skill in the art to combine the features of AAPA and Hadderman by adding the step of Hadderman regarding the ending of processing upon detecting a disconnection from a power supply. Both AAPA and Hadderman are directed towards peripheral card devices that may be inserted and removed from a computer system by a user, and as such are directed towards analogous subject matter. Additionally, both AAPA and Hadderman are concerned with the scenario in which such a device is removed from a computer system, as demonstrated by the mechanism in both inventions that detect such a removal. The teachings of Hadderman would improve the system of AAPA by ensuring that and pending processing is allowed to complete when the card is removed from the system. As would be recognized by one of ordinary skill in the art, such a step would ensure data integrity, and prevent errors.

Regarding claim 3, the combination of AAPA and Hadderman teaches the limitations of claim 1, and also teaches the starting up on a power supply circuit to supplement the operation power supply of the processing circuit [Fig. 1, independent power source 115, Fig. 4, step 415].

Regarding claim 4, AAPA teaches the monitoring terminal coupled to the first external terminal that is used to monitor the potential change at the first terminal [applicant's specification, page 1]:

"If an ATA card is inserted in the card slot and the corresponding terminals are connected to each other, the terminal in the card slot is grounded, then an interface circuit **in the card slot, which monitors the terminal**, detects the inserted card, thereby beginning supply of an operation power to the card. When the card is ejected, the corresponding terminals are disconnected, then the interface circuit in the card slot detects the supply voltage at the terminal in the card slot, thereby detecting the ejection of the card. The interface circuit in the card slot, when detecting such card ejection, stops the operation power supply to the card."

Regarding claim 6, AAPA teaches:

said first external terminal receives a first voltage when the processing circuit is active and said first external terminal is coupled to said second external terminal through a resistance element, and wherein said second external terminal receives a second voltage from the external apparatus, the polarity of said second voltage being opposite from that of said first voltage [applicant's specification, page 1]. More specifically, AAPA teaches a pulled-down and a pulled-up terminal in the card and card slot, respectively. When the terminals are connected, the card slot terminal is grounded, and power is supplied to the card. Additionally, a "pulled-down" and "pulled-up" terminal implies a pull-up or pull-down resistor used to connect the terminal to a voltage level.

Regarding claim 8, AAPA teaches that the first voltage is a supply voltage and said second voltage is a circuit ground voltage while said second external terminal is a ground source terminal.

Regarding claim 9, AAPA teaches the first external terminal is one of a plurality of ground terminals and said one of the ground terminals is connected to a power supply terminal through a resistance element [Fig. 1, 3, 5, Japanese Patent Application].

Regarding claim 10, AAPA and Hadderman teaches said processing circuit includes a non-volatile memory enabling information to be written/erased therein/therefrom electrically; and wherein said interface control circuit is a control circuit for controlling both of said external interface and said non-volatile memory [Hadderman, Fig. 1, DRAM^2].

Regarding claim 11, Hadderman teaches that ending processing adjusts threshold voltages of non-volatile memory cells so as to be set in a predetermined threshold voltage range during an erasure/write processing [Fig. 4, step 410].

Regarding claim 14, the combination of AAPA and Hadderman teaches [see claims 1, 3, 6, 8-11]:

a plurality of external terminals, each of which is attachable/detachable to/from its corresponding terminal of an external apparatus;

a first processing circuit coupled to said plurality of external terminals; a second processing circuit controlled by said first processing circuit;

and a resistance element used for connection between a first external terminal and a second external terminal among said plurality of external terminals, wherein said first external terminal receives a first voltage when said second processing circuit is active, wherein said second external terminal receives a second voltage, and wherein said first processing circuit,

when the system is removed from said external apparatus, detects a voltage change from said first voltage to said second voltage at said first external terminal before power supply from the external apparatus is shut off, then executes a processing in response to the detected voltage change.

Regarding claim 15, it would have been obvious to one of ordinary skill in the art for the first external terminal to be a reset terminal. Reset pins are commonly used in such systems.

Regarding claim 16, the combination of AAPA and Hadderman teaches the limitations of claim 14, and also teaches detecting a voltage change from a ground voltage to a supply voltage at the first external terminal [applicant's specification page 1].

Regarding claim 17, it would have been obvious to one of ordinary skill in the art for said first external terminal to be disposed so as to be disconnected from its corresponding terminal of the external apparatus earlier than other ground terminals when the system is removed from said external apparatus.

Regarding claim 18, the claim is rejected on similar grounds as claim 10.

Claims 2, 5, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Konishi et al., U.S. Patent No. 5,745,912.

Regarding claim 2, AAPA teaches:

a semiconductor processing system comprising an interface control circuit and a processing circuit, and attached to an external apparatus so as to receive an operation power supply therefrom, wherein said interface control circuit, when said system is removed from the external apparatus, detects a potential change that occurs at a first external terminal to be disconnected from a predetermined terminal of the external apparatus before the power supply

[2] Although DRAM is normally considered volatile, in this case the DRAM of Hadderman is equipped with a

from the external apparatus is shut off [applicant's specification, pages 1-2, "Background of the invention", also translated Patent Abstract, and Fig. 1, 3, 4, 5 of Japanese Patent Application].

AAPA does not teach the storing of a flag denoting an occurrence of a power supply shutoff.

Konishi teaches a memory card apparatus that stores a flag that denotes occurrence of a power supply shutoff [col. 4, lines 43-59].

It would have been obvious to one of ordinary skill in the art to combine the features of AAPA with Konishi by adding a flag that indicates a loss of power to AAPA, such as that taught by Konishi. Both AAPA and Konishi are directed towards removable peripheral card devices, and as such may be considered to be analogous subject matter. Additionally, Konishi addresses the scenario that is presented by AAPA – namely, removal of the peripheral card device that results in a loss of power supplied to the device. The addition of Konishi's teachings would improve AAPA by adding a means for detecting when an error has been introduced during a memory read/write operation by a sudden loss of power or removal of the device from an external apparatus [col. 3, lines 35-45].

Regarding claim 5, AAPA teaches:

said first external terminal receives a first voltage when the processing circuit is active and said first external terminal is coupled to said second external terminal through a resistance element, and wherein said second external terminal receives a second voltage from the external apparatus, the polarity of said second voltage being opposite from that of said first voltage [applicant's specification, page 1]. More specifically, AAPA teaches a pulled-down and a pulled-up terminal in the card and card slot, respectively. When the terminals are connected, the card slot terminal is grounded, and power is supplied to the card. Additionally, a "pulled-down" and

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data-retention mode, so it may be considered non-volatile.

"pulled-up" terminal implies a pull-up or pull-down resistor used to connect the terminal to a voltage level. Furthermore, it would have been obvious to one of ordinary skill in the art for the first external terminal to be a reset terminal. Reset pins are commonly used in such systems.

Regarding claim 7, AAPA teaches that the first voltage is a ground voltage and said second voltage is a supply voltage while said second external terminal is an external supply terminal.

Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Hadderman as applied to claim 10 above, and further in view of Konishi.

Regarding claim 12, AAPA/Hadderman does not teach the setting of a flag. Konishi teaches the setting of a flag in a location in link table that is associated with a particular memory location during a memory write operation [col. 6, lines 3-18].

It would have been obvious to one of ordinary skill in the art to combine the features of AAPA/Hadderman with Konishi by setting a flag associated with a memory location, such as that taught by Konishi. Both AAPA/Hadderman and Konishi are directed towards removable peripheral card devices, and as such may be considered to be analogous subject matter. Additionally, Konishi addresses the scenario that is presented by AAPA/Hadderman – namely, removal of the peripheral card device that results in a loss of power supplied to the device. The addition of Konishi's teachings would improve AAPA/Hadderman by adding a means for detecting when an error has been introduced at a particular memory location during a memory read/write operation by a sudden loss of power or removal of the device from an external apparatus [col. 3, lines 35-45].

Regarding claim 13, the AAPA/Hadderman/Konishi teaches that ending processing includes a completing processing for the current erasure/write processing for a non-volatile memory cell [col. 7, lines 7-10, Fig. 4, step 405].

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Evoy, U.S. Patent No. 6,062,480;

Yoshimura, U.S. Patent No. 6,724,678 B2;

Bass et al., U.S. Patent No. 6,041,375;

Davis, U.S. Patent No. 5,862,393.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ji H. Bae whose telephone number is 571-272-7181. The examiner can normally be reached on Monday-Friday, 10 am to 6:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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